High-Frequency Response of 100nm Integrated CMOS Transistors with High-K Gate Dielectrics

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I. Abstract

This paper reports, for the first time, the high-frequency response of NMOS and PMOS transistors in an integrated CMOS technology with 100 nm physical gate length and alternative gate dielectrics such as ZrO_2 and HfO_2 with TiN/PolySi gate electrode. It is shown that the dielectric constants of ZrO_2, HfO_2 and SiO_2 are invariant with respect to operating frequency at least up to 20 GHz. In addition, the cutoff frequency f_t of the 100 nm CMOS transistor test structures with ZrO_2 gate dielectric was measured to be equal to 46 GHz for NMOS and 47 GHz for PMOS. The corresponding f_t values for HfO_2 were 45 GHz for NMOS and 35 GHz for PMOS. High-K film transistors with 80nm physical gate lengths, 7 μm gate width and layout optimized for high frequency testing were also fabricated. The NMOS devices achieved an f_t of 83 GHz and an f_{max} of 35 GHz, while the PMOS yielded 41 GHz and 25 GHz respectively. These results are very similar to those of CMOS transistors with SiO_2 gate dielectric at similar physical gate lengths and widths. These results are very encouraging and suggest that high-K gate dielectrics can be used for high-frequency logic applications.

II. Introduction

There have been numerous reports on high-K gate dielectric materials in the literature [1-6]. The most commonly reported high-K materials are ZrO_2 [1-2], HfO_2 [3-4] and Al_2O_3 [5-6]. However, in these reports only DC and low-frequency device parameters are discussed with no information given on the high-frequency response of these new high-K materials. The high-frequency characteristics of high-K materials are very important for logic microprocessor applications. In this work, the focus is on the high-frequency response of ZrO_2 and HfO_2 gate dielectric. The equivalent oxide thickness (EOT) of the ZrO_2 and HfO_2 gate dielectrics are 2.1 nm and 1.4 nm respectively. It is found that under equivalent testing conditions no difference in the high frequency response is observed between the high-K samples and the SiO_2 control sample. Devices with optimized layouts for high frequency testing were also tested and found to exhibit good f_t and f_{max} parameters.

III. DC and Low-Frequency Characteristics

Integrated CMOS transistors with 100nm physical gate length and alternative gate stacks were fabricated with TiN/polySi (polySi on TiN) electrode. The gate dielectrics used were ZrO_2 and HfO_2 with EOT = 2.1 nm and 1.4 nm respectively. 100 nm CMOS transistors with thin SiO_2 (EOT = 1.2 nm) and TiN/PolySi electrode were also fabricated for reference. Both ZrO_2 and the HfO_2 sample showed similar DC and low-frequency device characteristics. The results from the HfO_2 sample and SiO_2 are compared here due to their similar EOT. Fig. 1-2 show the NMOS and PMOS I_d-V_d family of curves for the high-K and SiO_2 gate dielectrics respectively. Fig. 3-4 show the NMOS and PMOS sub-threshold characteristics of the high-K and SiO_2 gate dielectrics respectively. The NMOS and PMOS CV curves in inversion of the high-K and SiO_2 are shown in Fig. 5-6. The CV measurements were performed using the standard split CV technique on transistors. Fig. 7 shows the NMOS mobility of the high-K and SiO_2 compared to the universal mobility of Reference [7].

IV. High-Frequency Results and Discussion

There has been considerable speculation about the high frequency response of high-K dielectrics. Previously, no high frequency results have been reported on high-K dielectrics. The choice of test structure and methodology is extremely important. This paper presents a technique to examine high frequency behavior in a reliable manner that minimizes the impact of intrinsic resistance.

An 8510C network analyzer with high frequency ground-signal probes was used to characterize the transistors. The test structure is schematically illustrated in Figure 8. This structure has twenty 10 μm wide transistors connected in parallel. As a first step, the split C-V was measured from 1 MHz to 20 GHz. It was observed that the effective inversion capacitance decreased with frequency for high-K gate dielectrics and SiO_2 as shown in Fig. 9-10. This reduction in gate capacitance with respect to frequency is attributed to series resistance of the channel and the gate electrode [8]. These resistances, illustrated in the schematic shown in Fig. 11, prohibit determination of the dielectric constant from the high-frequency split C-V measurements. However this problem can be solved by measuring only the Miller capacitance (C_{ov}=C_{ox} at V_{gs}-V_{norm}=0) as a function of frequency of a long gate length transistor (1.0 μm). Use of the Miller capacitance eliminates the effect of channel resistance, while the long gate length minimizes the series resistance of the gate electrode. The Miller capacitance measurement allows the accurate determination of dielectric constant with respect to frequency as shown in Fig. 12. These results clearly show that the dielectric constants of ZrO_2, HfO_2 and SiO_2 are invariant with respect to operating frequency at least up to 20 GHz.

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S-parameters were also measured with optimal active bias applied to the test transistor to determine the cutoff frequency of the device shown in Fig. 8 with a gate length of 100 nm. These measurements yielded f_t of 45 GHz for NMOS and 47 GHz for PMOS in ZrO_2, while 45 GHz for NMOS and 35 GHz for PMOS in HfO_2. These f_t results are very similar to those of the control CMOS transistors with the SiO_2 gate oxide for similar physical gate lengths and layout structure.

The structure illustrated in Fig. 8 was not optimized for optimum high frequency performance parameters f_t and f_{max}. To evaluate these primary performance parameters, high-K devices with optimized structures were designed and fabricated as shown in Fig. 13. The S-parameters of the 80 nm gate length NMOS device measured at optimum conditions using 6 fingers of 7 µm gate width with single sided gate contact is shown in Fig. 14. The high-K NMOS devices achieved an f_t of 83 GHz and an f_{max} of 35 GHz while the high-K PMOS yielded 41 GHz and 25 GHz respectively. An examination of H_{21} for the high-K PMOS and NMOS devices (Fig. 15) yield a nearly ideal slope of 20 dB/dec, similar to SiO_2 devices. This is further indication of the healthy high frequency dielectric response of high-K dielectrics.

V. Summary

For the first time, the high-frequency response of high-K gate dielectrics in an integrated CMOS is reported. A TiN/PolySi gate electrode was used. It is shown that the dielectric constants of ZrO_2, HfO_2 and SiO_2 are invariant with respect to operating frequency at least up to 20 GHz. In addition, the cutoff frequency f_t of the 100 nm CMOS transistor test structures with ZrO_2 gate dielectric was measured to be equal to 46 GHz for NMOS and 47 GHz for PMOS. The corresponding f_t values for HfO_2 were 45 GHz for NMOS and 35 GHz for PMOS. High-K film transistors with 80 nm physical gate lengths, 7 µm gate width and layout optimized for high frequency testing were also fabricated. The NMOS devices achieved an f_t of 83 GHz and an f_{max} of 35 GHz, while the PMOS yielded 41 GHz and 25 GHz respectively. These high frequency parameter results are similar to those of the CMOS transistors with SiO_2 gate dielectric for similar physical gate lengths and widths. These results are very encouraging and suggest that high-K gate dielectrics are suitable for high performance microprocessor applications.

VI. References

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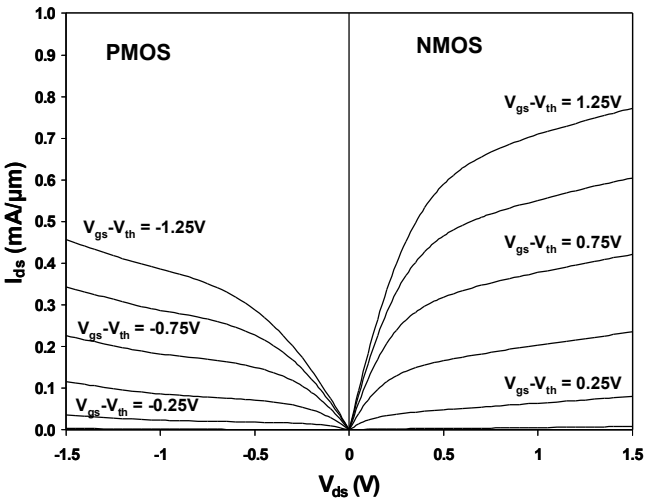

Figure 1: Family of curves for PMOS and NMOS for the high-K device with TiN/PolySi electrode. L_g =100nm.

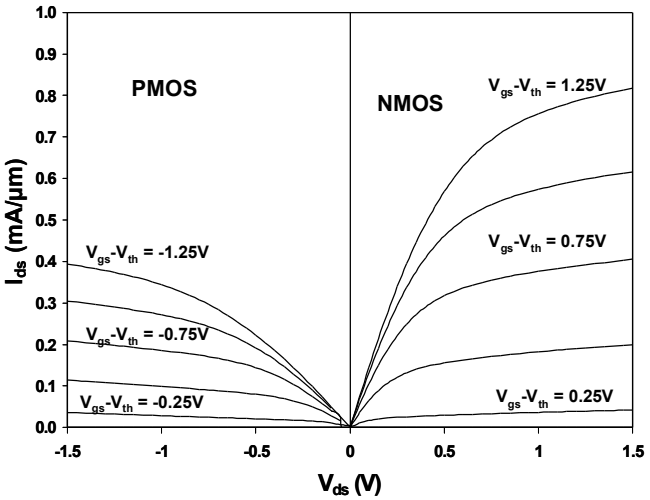

Figure 2: Family of curves for PMOS and NMOS for the SiO_2 device with TiN/PolySi electrode. L_g =100nm.

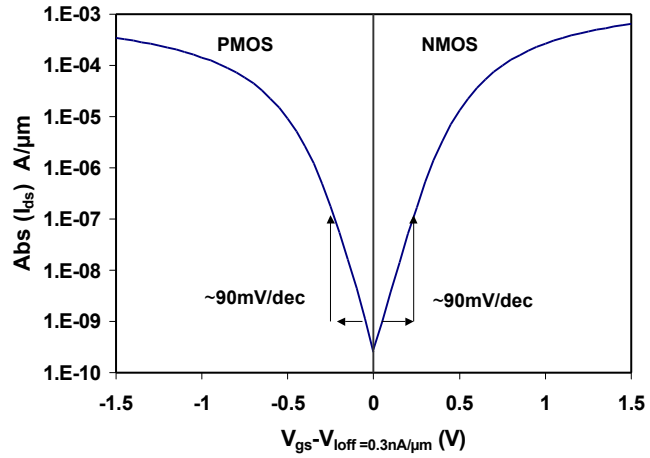

Figure 3: Subthreshold I-V curves for PMOS and NMOS for the high-K device with TiN/PolySi gate electrode at $|V_{ds}|$=1.5V. L_g =100nm.

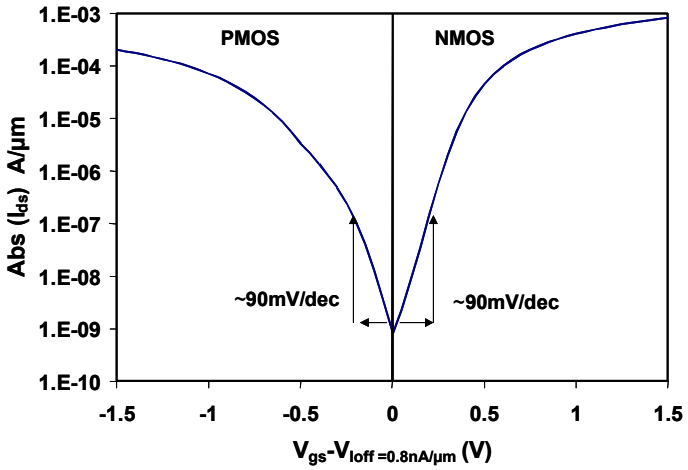

Figure 4: Subthreshold I-V curves for PMOS and NMOS for the SiO_2 device with TiN/PolySi gate electrode at $|V_{ds}|$=1.5V. L_g =100nm.

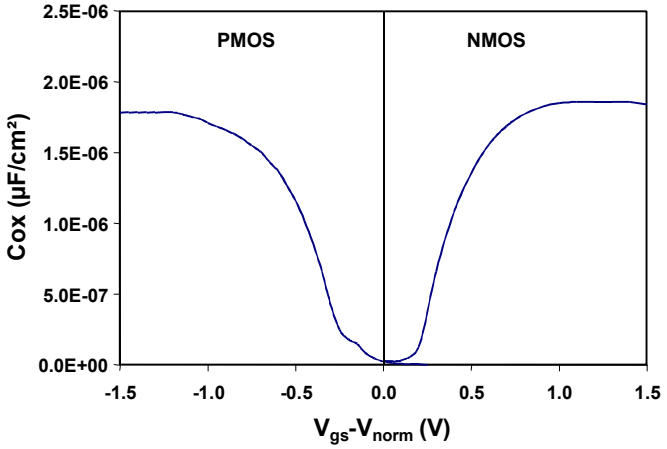

Figure 5: PMOS and NMOS inversion split C-V curves for the high-K devices.

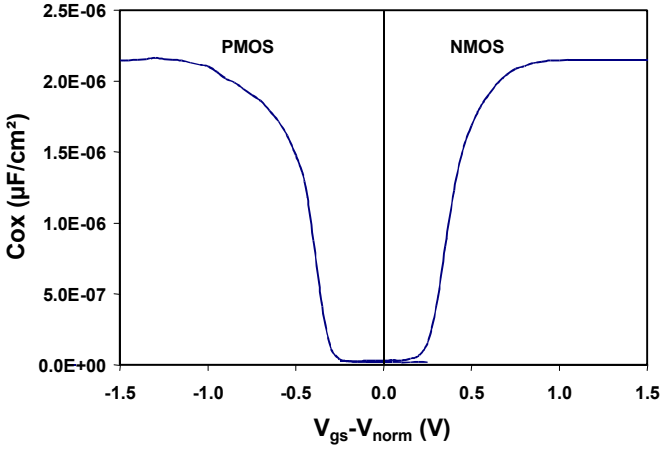

Figure 6: PMOS and NMOS inversion split C-V curves for the SiO_2 devices.

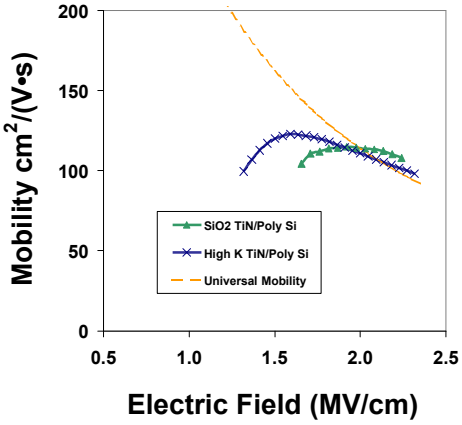

Figure 7: The NMOS effective high field mobility for the high-K and SiO_2.

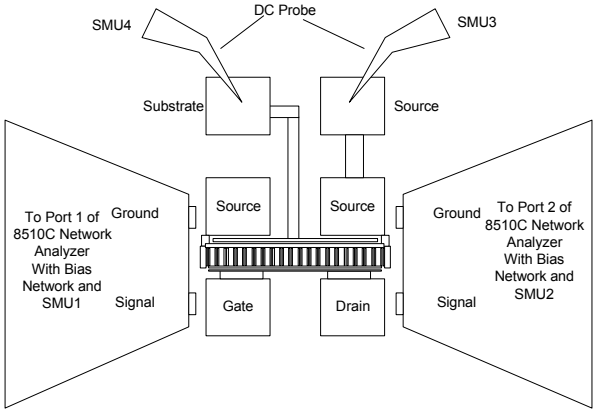

Figure 8: Test structure used for this experiment.

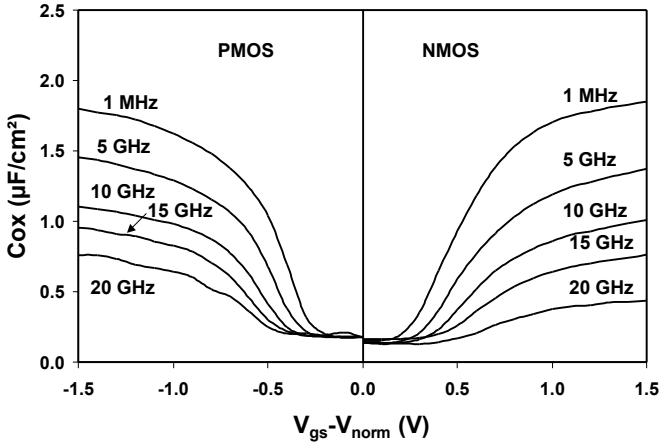

Figure 9: High Frequency split CV's of the high-K device. The Miller capacitance measured at V_{gs}-V_{norm} =0 is nearly invariant with respect to frequency. The physical gate length used for this measurement was one micron.

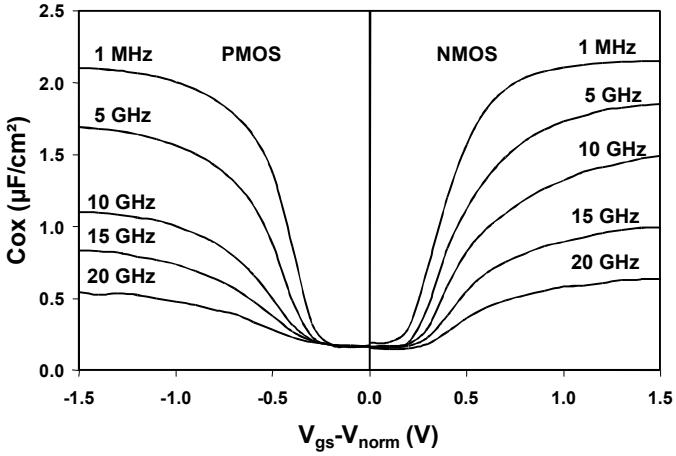

Figure 10: High Frequency split CV's of SiO_2 device. The Miller capacitance measured at V_{gs}-V_{norm} =0 is nearly invariant with respect to frequency. The physical gate length used for this measurement was one micron.

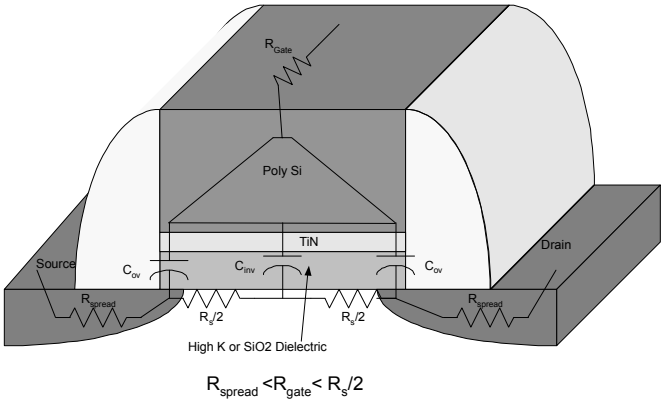

Figure 11: Schematic of the test transistor illustrating the various resistor components.

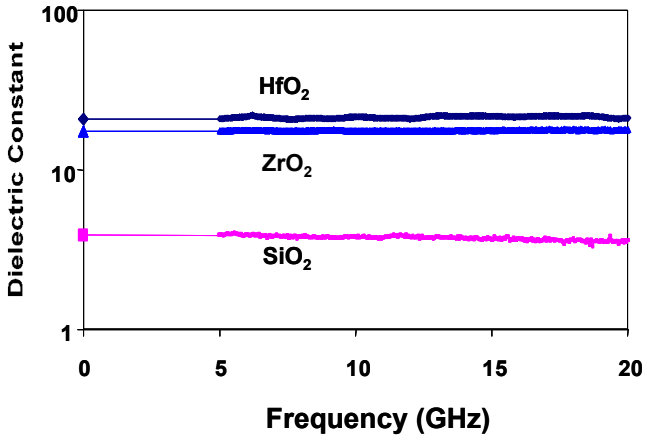

Figure 12: Dielectric constants from 5 to 20GHz evaluated with the NMOS Miller structure. No degradation in dielectric constant is observed for SiO_2, HfO_2 or ZrO_2.

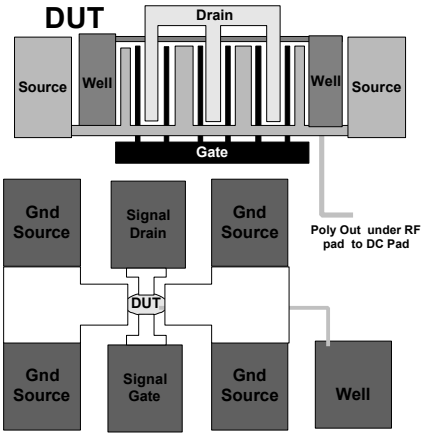

Figure 13: Optimized test structure used for this experiment.

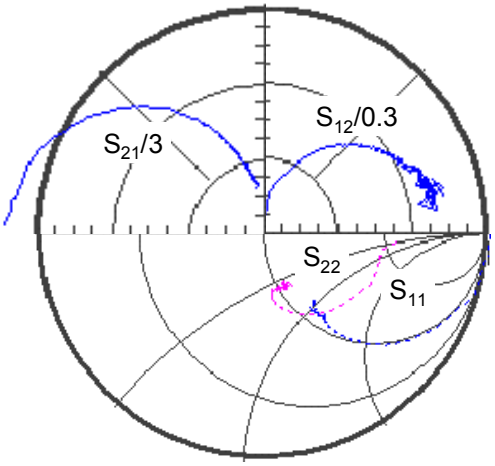

Figure 14: S-parameter data of an optimized high frequency NMOS test structure with high-K gate dielectric (L_g=80nm) swept from 0.25-50 GHz yields f_t of 83 Ghz.

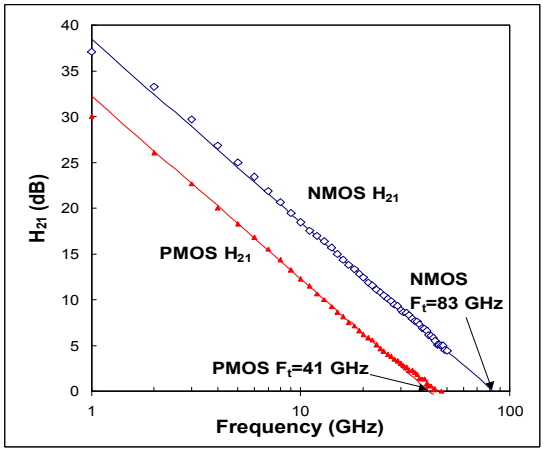

Figure 15: H_{21} vs. frequency of an optimized high frequency test structure with high-K gate dielectric (L_g=80nm). Note that the H_{21} parameter does not deviate significantly from the ideal 20dB/dec high frequency roll-off.